**AXI Test Procedures:**

|  |  |
| --- | --- |
| **Test** | **Corresponding Requirement** |
| RT\_1: All outgoing signals shall be set to ‘0’ if the following condition is met   * ‘S\_AXI\_ARESETN’ is ‘0’ | 1 |
| RT\_2: RSTATE shall be in wait\_for\_address\_valid if the below condition is met   * ‘S\_AXI\_ARREADY’ is ‘1’ | 2,3,4,5 |
| RT\_3:  Read\_enable shall be set to ‘1’, read\_address shall become ‘S\_AXI\_ADDR’, ‘S\_AXI\_ARREADY’ shall be set to ‘0’, READ\_SM shall transition from wait\_for\_address\_valid to wait\_for\_ack if both the below conditions are met   * ‘S\_AXI\_ARREADY’ is ‘1’ * ‘S\_AXI\_ARVALID’ is ‘1’ | 3 |
| RT\_4: ‘S\_AXI\_ARREADY’ shall be set to ‘0’ if the below condition is met   * RSTATE is not in wait\_for\_address\_valid | 3 |
| RT\_5: If ‘S\_AXI\_RVALID’ is ‘1’ it shall be set to ‘0’ if the following condition is met   * ‘S\_AXI\_RREADY’ is ‘1’ | 5 |
| RT\_6: RSTATE shall transition back to idle if the following conditions are met   * S\_AXI\_RREADY is ‘1’ * S\_AXI\_RVALID is ‘1’ * RSTATE is in wait\_master\_read\_ready | 5 |
| RT\_7: ‘S\_AXI\_ARREADY’ shall be set to ‘1’ if both the below conditions are met   * RSTATE is in idle * ‘S\_AXI\_ARESETN’ is ‘1’ | 2 |
| RT\_8: S\_AXI\_RVALID shall be set to ‘1’ if the below conditions are met   * Read\_ack is ‘1’ | 4 |
| RT\_9: S\_AXI\_RDATA shall become read\_data if the below condition is met   * Read\_ack is ‘1’ | 4 |
| WT\_1:  WSTATE shall be in idle state by default and when ‘S\_AXI\_ARESETN’ is ‘0’ | 13 |
| WT\_2:  ‘S\_AXI\_AWREADY’ shall be set to ‘1’ in ready state by default, and shall be set to ‘0’ synchronously and ‘S\_AXI\_AWADDR’ latched when the following conditions are met:   * ‘S\_AXI\_AWVALID’ is ‘1’ * ‘S\_AXI\_AWREADY’ is ‘1’ | 14, 15, 16 |
| WT\_3:  ‘S\_AXI\_WREADY’ shall be set to ‘1’ in ready state by default, and shall be set to ‘0’ synchronously and ‘S\_AXI\_WDATA’ latched when the following conditions are met:   * ‘S\_AXI\_WVALID’ is ‘1’ * ‘S\_AXI\_WREADY’ is ‘1’ | 17, 18, 19 |
| WT\_4:  ‘S\_AXI\_AWADDR’ and ‘S\_AXI\_WDATA’ shall be sent to register controller when the following are met:   * WSTATE is in write state. * ‘IntRdy’ is ‘1’ | 20 |
| WT\_5:  ‘S\_AXI\_BVALID’ shall be set to ‘1’ in response state by default, and shall be set to ‘0’ synchronously and error info sent on ‘S\_AXI\_BRESP’ line when the following conditions are met:   * ‘S\_AXI\_BVALID’ is ‘1’ * ‘S\_AXI\_BREADY’ is ‘1’ | 21, 22, 23 |